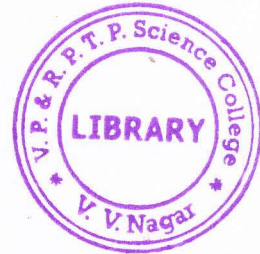


V. P. & R. P. T. P. Science College
First Internal Exam
US04CELE-02

11/03/19
3:00 p.m to 5.00 p.m.
Total Marks 50

08

Q.1 Multiple Choice Questions:



1. Parity checker is used for checking
 - i) 1 bit error
 - ii) 2 bit error
 - iii) Multiple bit error
2. If propagation delay is low
 - i) The circuit is faster
 - ii) The circuit is slow
 - iii) None of above
3. Schmitt Trigger circuit is
 - i) Astable multivibrator
 - ii) Bistable multivibrator
 - iii) Monostable multivibrator
4. RC differentiation circuit used in Edge triggered FF has on time
 - i) Equal to Clock Pulse
 - ii) Greater than Clock Pulse
 - iii) Less than Clock Pulse
5. Circuit is very complex in case of
 - i) Serial Counter
 - ii) Parallel Counter
 - iii) Combinational Counter
6. A counter using 5 FFs will have total number of ----- states
 - i) 16
 - ii) 32
 - iii) 5
7. In order to construct down counter, FF needs to be triggered from
 - i) True side of o/p of previous FF
 - ii) False side of o/p of previous FF
 - iii) Clock pulse
8. Shift counter is used to shift the data in
 - i) Cyclic order
 - ii) Non-cyclic order
 - iii) Random order

Q.2 Answer any five questions in short.

10

1. Define Fan –in and Fan out of circuit.
2. State logic specifications of LSTTL NAND gate.
3. What are advantages of D Flip Flop over RS Flip Flop?

4. What is RC differentiation?
5. What is the advantage of combinational counter?
6. Draw circuit for Mod 5 Synchronous Counter?
7. Draw decoding gates for 0 and 9 of decade counter.
8. Draw combine circuit of Up/Down counter.

Q.3 Describe any two applications of X-OR gate. 08

OR

Q.3 Describe in detail working of TTL NAND gate with neat diagram. 08

Q.4 Describe in detail Edge triggered D Flip Flop. 08

OR

Q.4 Describe fully Schmitt Trigger circuit. 08

Q.5 Explain working of Mod 8 ripple counter. 08

OR

Q.5 Explain working of Mod 5 combinational counter. 08



*****BEST OF LUCK *****