V. P. & R. P. T. P. Science College
First Internal Exam
US04CELE-02

17/03/16
3:00 p.m to 4.30 p.m.
Total Marks 25

Q.1 Multiple Choice Questions: **03**

1. Pairity checker is used for checking
   i) 1 bit error
   ii) 2 bit error
   iii) Multiple bit error
   iv) None of the above
2. In J K Flip Flop, J=K=1, then
   i) Q=1
   ii) Q=forbidden state
   iii) Q=toggle
   iv) Last state
3. Delay time is less in case of
   i) Serial Counter
   ii) Parallel Counter
   iii) Combinational Counter
   iv) None of the above

Q. 2 Answer any two questions in short. **04**

1. Define Fan in and Fan out of circuit.
2. What are advantages of D Flip Flop over RS Flip Flop?
3. What is the advantage of combinational counter?

Q.3 Describe any two applications of X-OR gate. 06

OR

Q.3 Describe in detail working of TTL NAND gate with neat diagram. 06

Q.4 Describe in detail Edge triggered D Flip Flop. 06

OR

Q.4 Describe fully Schmitt Trigger circuit. 06

Q.5 Explain working of 8bit Asynchronous counter. Draw waveform diagram also. 06

OR

Q.5 Explain working of Mod 5 Asynchronous counter. Draw waveform diagram also. 06

**********BEST OF LUCK **********