V. P. & R. P. T. P. Science College First Internal Exam US04CELE-02

17/03/15 10.30 a.m to 12.00 noon Total Marks 25

Q.1	Multiple Choice Questions:	03
1.	The output of X-OR gate is high	
	I. When both the inputs are high	
	II. When both the inputs are low	
	III. When both the inputs are complementary	
	IV. None of the above	
2.	In J K Flip Flop, J=K=1, then	
	I. Q=1	
	II. Q=forbidden state	
	III. Q=toggle	
	IV. Last state	
3.	Delay time is more in case of	
	I. Serial Counter	
	II. Parallel Counter	
	III. Combinational Counter	
	IV. None of the above	
Q. 2	Answer any three questions in short.	04
	 Define Fan in and Fan out of Circuit. What are advantages of D Flip Flop over RS Flip Flop? What is the advantage and disadvantage of serial counter? 	
Q.3	Describe any three applications of X-OR gate.	06
	OR	
Q.3 I	Describe in detail working of TTL NAND gate with logic specifications.	06
Q.4	Describe in detail Edge triggered D Flip Flop.	06
	OR	
Q.4	Describe fully Schmitt Trigger circuit.	06
Q.5	Explain working of 8bit Asynchronous counter. Draw waveform diagram also. OR	06
Q.5	Explain working of Mod 6 parallel counter. Draw waveform diagram also.	06
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