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SARDAR PATEL UNIVERSITY
B.Sc. IV Semester
Course Code: US04CELE22
Instrumentation and Digital Electronics
Date: 11/04/2022, Time: 3:00 to 5:00 pm

TOTAL MARKS 70

Q. 1 Multiple Choice Questions: **10**

1. One can construct Binary to Gray convertor using
   (i) AND gate
   (ii) OR gate
   (iii) XOR gate
   (iv) NAND gate
2. The Full adder circuit can add
   (i) Two bits at a time
   (ii) Three bits at a time
   (iii) Multiple bits at a time
   (iv) None of the above
3. RC differentiation circuit used in Edge triggered FF has on time
   (i) Equal to Clock Pulse
   (ii) Greater than Clock Pulse
   (iii) Less than Clock Pulse
   (iv) Twice the clock pulse
4. RC differentiation circuit is used to generate _____ from clock pulses
   (i) Spikes
   (ii) Ractangular wave
   (iii) Square wave
   (iv) Triangular wave
5. PRESET and CLEAR are called
   (i) Synchronous Input
   (ii) Asynchronous input
   (iii) Serial input
   (iv) None of the above
6. The gate used for feedback in Counters is
   (i) AND Gate
   (ii) OR Gate
   (iii) NAND Gate
   (iv) XOR Gate
7. In order to count 32 states ---------- in ripple counter
   (i) 4 FFs are needed
   (ii) 3 FFs are needed
   (iii) 2 FFS are needed
   (iv) 5 FFs are needed
8. In order to construct down counter, FF needs to be triggered from
   (i) True side of o/p of previous FF
   (ii) False side of o/p of previous FF
   (iii) Clock pulse
   (iv) None of the above

P.T.O.

9. Binary decade counter counts
   (i) 10 states
   (ii) 16 states
   (iii) 4 states
   (iv) 20 states
10. The decoding AND gate, to decode 15 will have input as
   (i) $\overline{D}\overline{C}\overline{B}A$
   (ii) $\overline{D}\overline{C}\overline{B}\overline{A}$
   (iii) $\overline{D}\overline{C}BA$
   (iv) $DCBA$

Q2: True or False **8**

1. The Half adder circuit can add two bits at a time.
2. Pairity checker is used for checking 2-bit error.
3. Toggle means complement of previous state.
4. Flip Flop is a Bistable multivibrator.
5. A counter is a circuit that counts number of clock pulses that hit the Counter.
6. Counters are generally made using JK Flipflop.
7. BCD 2421 counter has 6 illegal states.
8. In order to construct down counter, FF needs to be triggered from True side of o/p of previous FF.

Q3: Answer any 10 questions out of 12 questions briefly. **20**

1. List the logic specifications of a logic circuit.
2. Draw Full Adder circuit.
3. Write logic specifications for LSTTL NAND gate.
4. What is advantage of D Flip Flop over RS Flip Flop?
5. List applications of Schmitt trigger circuit.
6. Draw circuit of RS Flip Flop using NOR gate.
7. What is the advantage of combinational counter?
8. List different names given to serial counter.
9. What is the advantage and disadvantage of serial counter?
10. Draw decoding gate for states 0 and 12 of decade counter.
11. Draw combined circuit of UP/Down counter.
12. How many states are omitted in BCD 2421 counter? List them.

Q4: Answer any 4 questions out of 8 questions elaborately. **32**

1. Describe working of TTL NAND gate with neat diagram.
2. Describe any two applications of X-OR gate.
3. Describe working of Edge Triggered D Flipflop.
4. Explain in detail working of Astable multivibrator with neat diagram.
5. Explain working of 3-bit Serial counter.
6. Explain working of Mod 8 Parallel counter.
7. Explain working 3 stage shift counter.
8. Explain in detail Up/Down counter.

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