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Unit - 3

Basic FET Circuits

Introduction

There are three basic FET circuit configurations: common source, common drain, and common gate. These are similar to the bipolar transistor common emitter, common collector, and common base circuits, respectively. The common source circuit is capable of voltage amplification and it has a very high input impedance. The common drain circuit is a buffer amplifier, with approximately unity voltage gain, very high input impedance, and low output impedance. The common gate circuit has voltage gain, low input impedance, and excellent high-frequency performance.

10-1 Common Source Circuit

The circuit of a common source amplifier is illustrated in Fig. 10-1. The circuit shown employs potential divider bias and uses bypass capacitor C_2 to eliminate ac degeneration. The signal source (voltage v_i with source resistance r_i) is connected to the FET gate via coupling capacitor C_1 . Capacitor C_3 couples external load resistor R_L to the drain terminal. The circuit is a single-stage amplifier, with input and output terminals at the coupling capacitors, as illustrated.

Note the polarity of the capacitors in Fig. 10-1. As discussed in Section 5-1, the negative terminal of each (polarized) capacitor must always be at a lower dc potential than the positive terminal. Incorrectly connected capacitors can affect the bias conditions and ac performance of the circuit.

For ac considerations, bypass capacitor C_2 in Figure 10-1 effectively ties the FET source terminal to ground level. Thus, all of the input voltage v_i is developed across the gate-source terminals. When the input voltage increases and decreases, the resultant change in V_{GS} causes the I_D level to increase and decrease correspondingly. The change in I_D alters the voltage drop across drain resistor R_D . This variation in V_{RD} constitutes the ac output voltage v_o .

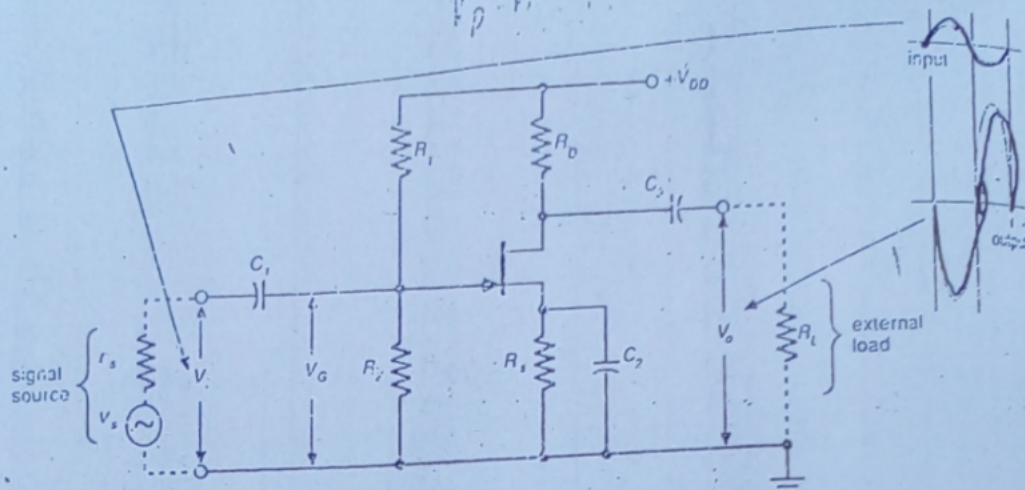
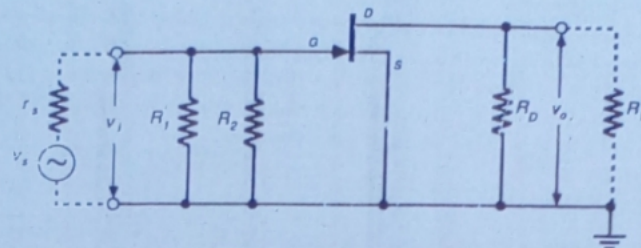


Figure 10-1 Common source amplifier circuit, showing the signal capacitor-coupled to the FET gate and the load capacitor-coupled to the drain terminal.

The phase relationship between the circuit input and output voltage can be determined by considering the effect of a positive-going input signal. When v_i increases in a positive direction, it reduces the negative gate-source voltage $-V_{GS}$. The reduction in $-V_{GS}$ raises the level of I_D and consequently increases the voltage drop across R_D . Since $V_D = V_{DD} - I_D R_D$, the increase in I_D results in a drop in drain (output) voltage V_D . Thus, as v_i increases in a positive direction, v_o goes in a negative direction. Similarly, when v_i goes negative, the resultant increase in $-V_{GS}$ reduces the I_D level which, in turn, reduces the voltage drop across R_D and produces a positive-going output voltage v_o . Thus, the amplifier output voltage is 180° out of phase with the input voltage. This phase relationship is illustrated by the waveforms in Fig. 10-1.

The voltage amplification, or gain, of the circuit is $A_v = v_o/v_i$. A_v depends upon R_D and R_L , and upon the FET parameters. Equations for voltage gain, input impedance, output impedance, etc., can be determined by ac analysis of the circuit.

The first step in ac analysis of the common source circuit is to draw the ac equivalent circuit. This is done by replacing the capacitors with short circuits, exactly as was done for ac analysis of bipolar circuits in Chapter 5. Also, since the supply voltage V_{DD} remains constant, it must be treated as another ac short circuit. This means that the $+V_{DD}$ terminal is at the same ac potential as ground. In the ac equivalent circuit in Fig. 10-2(a), R_1 is shown connected between the FET gate and ground, so that R_1 and R_2 are in parallel. Similarly, R_D appears across the transistor drain terminal and ground. When an external load resistance R_L is present, R_D and R_L are in parallel for ac considerations.



(a) Common source ac equivalent circuit

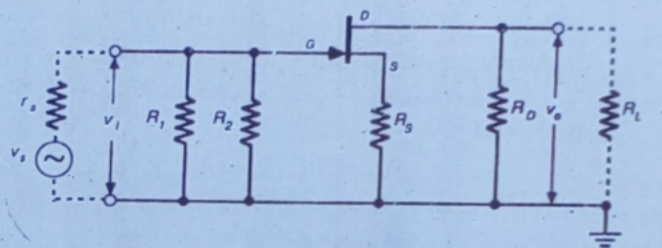
(b) ac equivalent circuit for common source amplifier with an unbypassed source resistor R_s

Figure 10-2 The ac equivalent circuit for a common source circuit is drawn by replacing all capacitors with short circuits. Supply voltage V_{DD} must also be treated as an ac short circuit.

Figure 10-2(a) shows that the circuit input voltage is developed across the FET gate and source terminals. The output is taken from the drain and source terminals. Since the source is common to both input and output, the circuit is designated *common-source*, or sometimes *grounded-source*.

Some common source circuits may not include bypass capacitor C_2 . Alternatively, the source resistance may be made up of two series-connected resistors, with C_2 bypassing only one of the two. In any situation where an unbypassed source resistor R_s exists, R_s must be included in the ac equivalent circuit [see Fig. 10-2(b)].

10-2 Ac Analysis of Common Source Circuit

Equivalent Circuit

The complete ac equivalent circuit for the common source amplifier is drawn by substituting the FET equivalent circuit (from Fig. 8-14) into the circuit of Fig. 10-2(a). The complete common source ac equivalent circuit is shown in

Fig. 10-3. As mentioned in the previous section, when the circuit contains an unbypassed source resistor R_S , R_S must be included in the equivalent circuit. The complete ac equivalent circuit for this situation is shown in Fig. 10-4. In Figs. 10-3 and 10-4, the current direction and voltage polarities are those that would occur as the input voltage goes positive.

Input Impedance

Looking into the gate and source terminals in Fig. 10-3, the resistance seen is the gate-source junction reverse resistance R_{GS} . Therefore, the device input impedance is

$$Z_g = R_{GS} \quad (10-1)$$

From Section 8-4, a typical value of R_{GS} might be $10^9 \Omega$.

When an unbypassed source resistor is included (Fig. 10-4), an equation for Z_g must be derived. Thus,

$$\begin{aligned} v_i &= V_{gs} + I_d R_S \\ &= V_{gs} + g_m V_{gs} R_S \\ &= V_{gs} (1 + g_m R_S) \end{aligned}$$

or

$$V_{gs} = \frac{v_i}{1 + g_m R_S}$$

and

$$I_i = \frac{V_{gs}}{R_{GS}} = \frac{v_i}{R_{GS} (1 + g_m R_S)}$$

So

$$\begin{aligned} Z_g &= \frac{v_i}{I_i} \\ Z_g &= R_{GS} (1 + g_m R_S) \end{aligned} \quad (10-2)$$

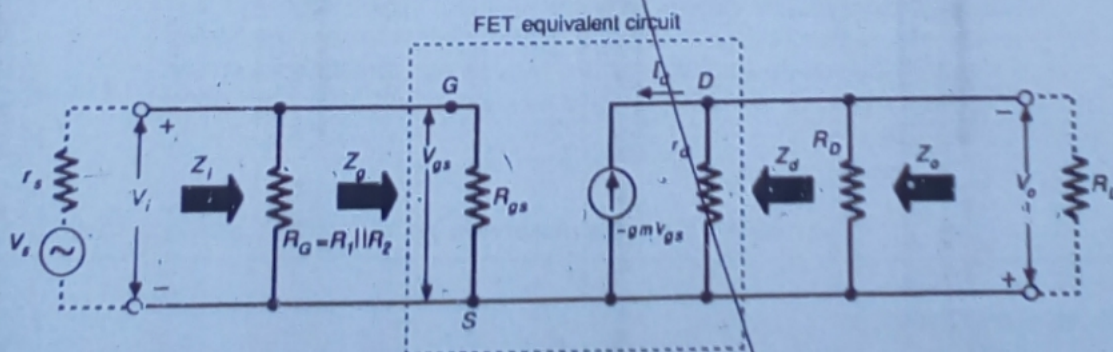


Figure 10-3 The complete equivalent circuit for a common source amplifier is drawn by substituting the FET equivalent circuit into the ac equivalent circuit of Fig. 10-2(a).

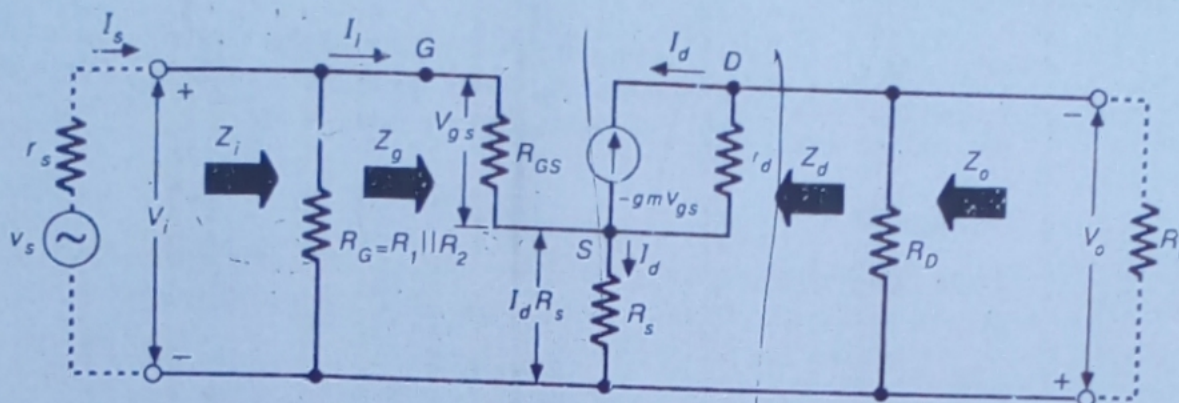


Figure 10-4 An unbypassed source resistor (R_S in Fig. 10-2(b)) must be included in series with the FET source terminal in the complete ac equivalent circuit for the amplifier.

With $g_m = 5 \text{ mA/V}$ and $R_S = 5 \text{ k}\Omega$, $Z_g = 26 R_{GS}$. This value is extremely large, and when the bias resistors are placed in parallel with Z_g (see below), it might seem not worth the trouble of working out the equation. However, as already stated, one of the most important properties of the field effect transistor is its high input impedance. In circumstances where it is necessary to achieve the highest possible input impedance, the signal source might be connected directly in series with the gate terminal, instead of being capacitor-coupled between the gate and ground. In this situation, it may be important to be able to calculate Z_g .

Equations 10-1 and 10-2 give the input impedance to the FET gate terminal. The circuit input impedance is $R_G \parallel Z_g$ (see Figs. 10-3 and 10-4). That is,

$$Z_i = R_G \parallel Z_g \quad (10-3)$$

Because Z_g is normally very much greater than R_G , the circuit input impedance is almost always taken to be R_G . (An exception to this is discussed above.) The input impedance for most FET circuits can be determined simply by reading the resistance value of R_G .

Output Impedance

Looking into the drain and source terminals, the large drain resistance r_d is seen. Thus,

$$Z_d \approx r_d \quad (10-4)$$

Z_d is the device output impedance; the circuit output impedance is R_D in parallel with Z_d :

$$Z_o = R_D \parallel Z_d \quad (10-5)$$

Typically, $r_d = 100 \text{ k}\Omega$, and since it is usually the case that $r_d \gg R_D$, the circuit output impedance is taken to be R_D . Once again, the Z_o of the circuit can be determined simply by reading the resistance value of R_D .

Voltage Gain

From Fig. 10-3,

$$v_o = I_d (r_d \parallel R_D \parallel R_L)$$

and

$$I_d = -g_m v_i$$

Therefore,

$$v_o = -g_m v_i (r_d \parallel R_D \parallel R_L)$$

and

$$A_v = \frac{v_o}{v_i}$$

$$A_v = -g_m (r_d \parallel R_D \parallel R_L) \quad (10-6)$$

Usually,

$$r_d \gg R_D \parallel R_L$$

giving

$$A_v \approx -g_m (R_D \parallel R_L) \quad (10-7)$$

The minus sign indicates that v_o is 180° out of phase with v_i . (When v_i increases, v_o decreases, and vice versa.) It is seen that the voltage gain of a common source amplifier is directly proportional to the g_m of the FET. If the typical values of g_m , R_D , and R_L are known, the voltage gain of any circuit can be very quickly estimated. For $g_m = 5 \text{ mA/V}$, $R_D = 5 \text{ k}\Omega$, and $R_L = 100 \text{ k}\Omega$, a typical common source circuit voltage gain might be -25 . This is about one-tenth the voltage gain that may be expected with a bipolar transistor common emitter circuit. *Low voltage gain is the major disadvantage of JFET circuits*, compared to bipolar transistor circuits. The same is generally true of MOSFET circuits, but V-MOSFETs have g_m values around 2000 mA/V , so large voltage gains should be possible. However, these devices are not suitable for use in small-signal amplifiers, because they need relatively large drain currents. They are usually employed at the output of power amplifiers, which have very low resistance loads.

If R_S is unbypassed, as in Fig. 10-4, then, from the previous input impedance calculation,

$$v_i = V_{gs} (1 + g_m R_S)$$

Neglecting r_d ,

$$v_o \approx I_d (R_D \parallel R_L)$$

$$= -g_m V_{gs} (R_D \parallel R_L)$$

Also

$$A_v = \frac{v_o}{v_i}$$

$$A_v = \frac{-g_m(R_D \parallel R_L)}{1 + g_m R_S} \quad (10-8)$$

Thus,

$$g_m R_S \gg 1$$

then

$$A_v \approx \frac{-(R_D \parallel R_L)}{R_S} \quad (10-9)$$

Once again, the voltage gain of a circuit can be estimated just by looking to see the resistor values. If $R_D = 5 \text{ k}\Omega$, $R_L = 100 \text{ k}\Omega$, and $R_S = 5 \text{ k}\Omega$, then $A_v \approx -1$.

The common source circuit in Fig. 10-5 (the bias circuit designed in Example 9-7) uses a 2N5457 JFET. Using the typical FET parameter specifications, calculate Z_i , Z_o , and A_v .

Example 10-1

Solution

From the 2N5457 data sheet in Appendix 1-8,

$$r_d = \frac{1}{Y_{os}} = \frac{1}{10 \mu\text{S}} = 100 \text{ k}\Omega$$

and

$$g_m = Y_{fs} = 3000 \mu\text{S} = 3 \text{ mA/V}$$

$V_D \equiv V_{DD}$
 $Z_o \parallel R_D$

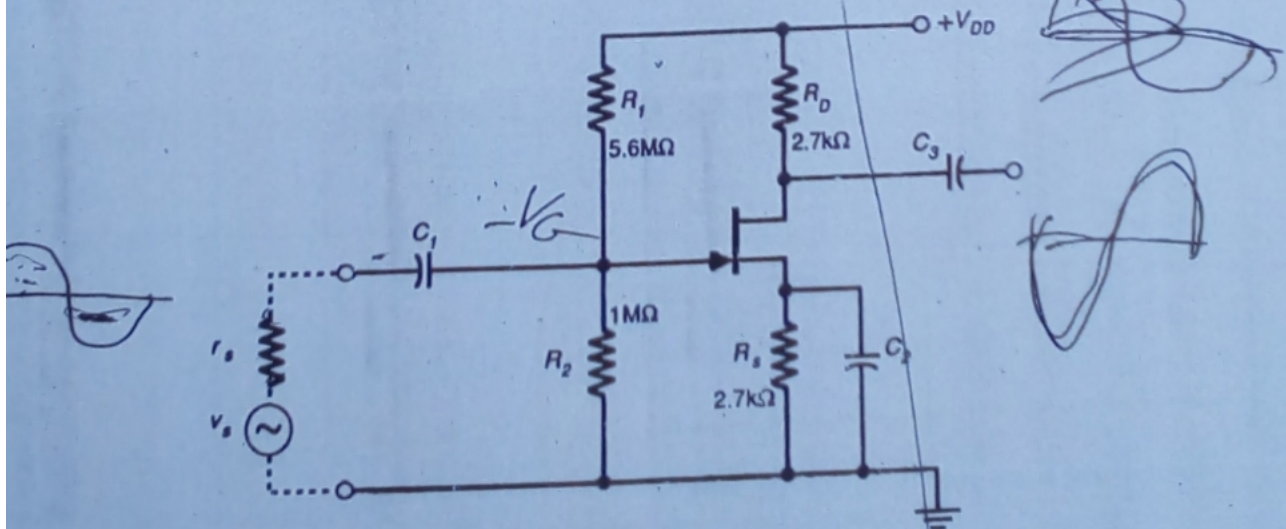


Figure 10-5 Common source circuit for Example 10-1.

From Eq. 10-3,

$$\begin{aligned} Z_i &= R_G = R_1 \parallel R_2 \\ &= 1 \text{ M}\Omega \parallel 5.6 \text{ M}\Omega = 848 \text{ k}\Omega \end{aligned}$$

From Eq. 10-5,

$$\begin{aligned} Z_o &= R_D \parallel r_d \\ &= 2.7 \text{ k}\Omega \parallel 100 \text{ k}\Omega = 2.63 \text{ k}\Omega \end{aligned}$$

From Eq. 10-6,

$$\begin{aligned} A_v &= g_m (r_d \parallel R_D) \\ &= -[3 \text{ mA/V} (100 \text{ k}\Omega \parallel 2.7 \text{ k}\Omega)] \\ &\approx -7.9 \end{aligned}$$

From Eq. 10-7,

$$\begin{aligned} A_v &\approx -\bar{g}_m R_D = -(3 \text{ mA/V} \times 2.7 \text{ k}\Omega) \\ &= -8.1 \end{aligned}$$

Example 10-2

Determine the voltage gain of the circuit in Example 10-1, (a) when a $1 \text{ k}\Omega$ unbypassed resistor is connected in series with the FET source terminal, (b) with R_S completely bypassed and an external load resistor of $R_L = 10 \text{ k}\Omega$ capacitor-coupled to the circuit output.

Solution

(a) From Eq. 10-8,

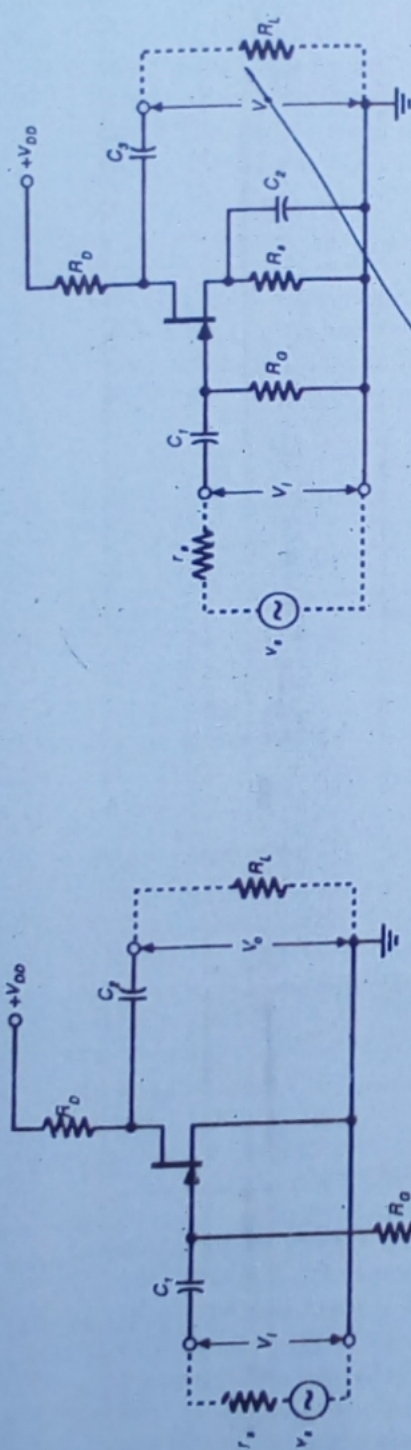
$$\begin{aligned} A_v &= \frac{-g_m R_D}{1 + g_m R_S} \\ &= \frac{-(3 \text{ mA/V} \times 2.7 \text{ k}\Omega)}{1 + (3 \text{ mA/V} \times 1 \text{ k}\Omega)} \\ &\approx -2 \end{aligned}$$

(b) From Eq. 10-6,

$$\begin{aligned} A_v &\approx -g_m (r_d \parallel R_D \parallel R_L) \\ &= -3 \text{ mA/V} (100 \text{ k}\Omega \parallel 2.7 \text{ k}\Omega \parallel 10 \text{ k}\Omega) \\ &= -6.2 \end{aligned}$$

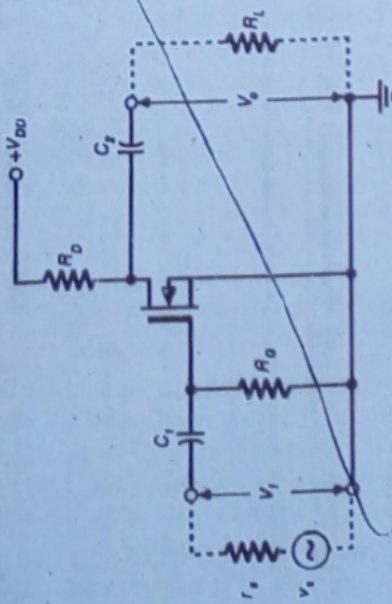
10-3 More Common Source Circuits

Common source circuits using fixed voltage bias and self-bias are illustrated in Fig. 10-6(a), (b), and (c). Like the V_{DD} terminal, the gate bias voltage terminal in Fig. 10-6(a) is considered an ac ground. Consequently, the ac equivalent

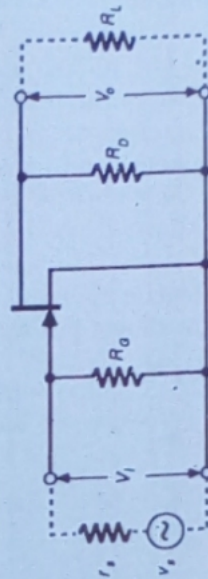


(a) Common source circuit using fixed voltage bias

(b) Common source circuit using self bias



(c) MOSFET Common source circuit using fixed voltage bias



(d) ac equivalent circuit for circuits (a), (b), and (c)

Figure 10-6 Common source circuits and their ac equivalent using fixed voltage bias and self-bias. The ac performance equations for these circuits are the same as those derived for the circuit using potential divider bias.

circuit in Fig. 10-6(d) applies to all three circuits. The presence of only one bias resistor in these circuits makes $Z_i = R_G$. Otherwise the ac performance equations are those derived in Section 10-2. In the case of a self-bias circuit with an unbypassed source resistor, the performance equations are the same as those derived for the equivalent circuit in Fig. 10-4.

Example 10-3

Calculate the input impedance, output impedance, and voltage gain for the circuit shown in Fig. 10-6(b). The component values are $R_G = 390 \text{ k}\Omega$, $R_D = 4.7 \text{ k}\Omega$, $R_S = 2.7 \text{ k}\Omega$, $R_L = 68 \text{ k}\Omega$. The transistor parameters are $g_m = 4000 \text{ }\mu\text{S}$ and $r_d = 80 \text{ k}\Omega$. Also, determine the voltage gain when C_2 is absent.

Solution

$$Z_i = R_G = 390 \text{ k}\Omega$$

$$\begin{aligned} Z_o &= r_d \parallel R_D \\ &= 80 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \\ &\approx 4.4 \text{ k}\Omega \end{aligned}$$

From Eq. 10-6,

$$\begin{aligned} A_v &\approx g_m (r_d \parallel R_D \parallel R_L) \\ &= -4000 \text{ }\mu\text{S} (80 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel 68 \text{ k}\Omega) \\ &= -16.7 \end{aligned}$$

From Eq. 10-8,

$$\begin{aligned} A_v &= \frac{-g_m (R_D \parallel R_L)}{1 + g_m R_S} \\ &= \frac{-[4000 \text{ }\mu\text{S} (4.7 \text{ k}\Omega \parallel 68 \text{ k}\Omega)]}{1 + (4000 \text{ }\mu\text{S} \times 2.7 \text{ k}\Omega)} \\ &\approx -1.5 \end{aligned}$$

10-4 Common Drain Circuit

In the common drain circuit in Fig. 10-7, the output voltage is developed across source resistor R_S . External load resistor R_L is capacitor-coupled to the source terminal of the FET, and gate bias voltage V_G is derived from V_{DD} by means of potential divider R_1 and R_2 . So the circuit employs potential divider bias. No resistor is connected in series with the drain terminal, and no source bypass capacitor is employed.

To understand the operation of the common drain circuit, note that (as in any potential divider bias circuit) V_G is a constant quantity. The source

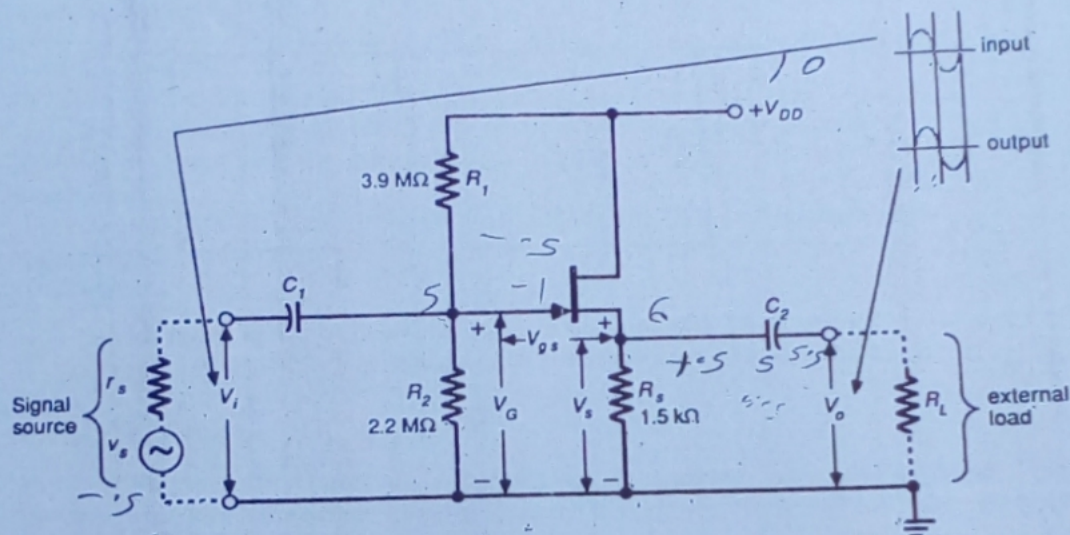


Figure 10-7 Common drain circuit, also known as a source follower. The input voltage is applied to the FET gate, and the output is taken from the source terminal.

voltage is $V_S = V_G + V_{GS}$. When a signal is applied to the FET gate via C_1 , V_G is increased and decreased as the signal goes positive and negative, respectively. Also, V_{GS} remains substantially constant, and because $V_S = V_G + V_{GS}$, the source voltage V_S increases by approximately 0.5 V when v_i increases by 0.5 V. Similarly, when the input goes to -0.5 V, V_S decreases by approximately 0.5 V. Since the FET source is the output terminal, it is seen that the output voltage from a common drain circuit is (approximately) the same as the input voltage. Thus, the common drain circuit can be said to have unity voltage gain. AC analysis of the common drain circuit demonstrates that v_o is slightly smaller than v_i .

Because the output voltage at the FET source terminal follows changes in the signal voltage applied to the gate, the common drain circuit is also known as a *source follower*.

As in the case of other semiconductor circuits, the supply voltage and coupling capacitors in Fig. 10-7 must be replaced with short circuits in order to study the ac performance. This gives the common drain ac equivalent circuit in Fig. 10-8. The input terminals of the ac equivalent circuit are gate and drain, and the output terminals are source and drain. The drain terminal is common to both input and output, so the circuit is named *common drain* or *grounded drain*.

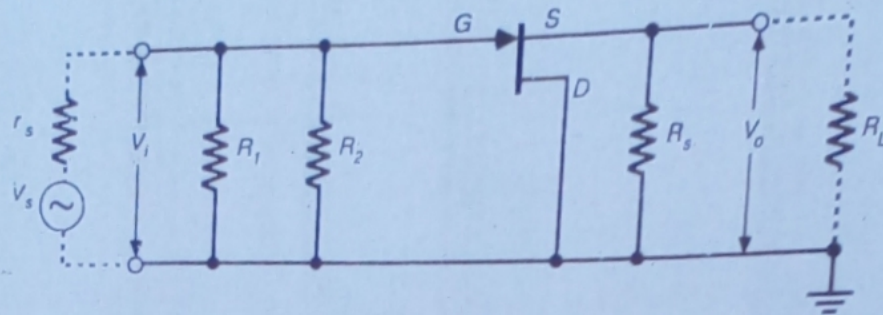


Figure 10-8 The common drain ac equivalent circuit is drawn by replacing supply voltage V_{DD} and all capacitors with short circuits.

10-5 Ac Analysis of Common Drain Circuit

Equivalent Circuit

The complete ac equivalent circuit for the common drain amplifier is drawn by substituting the FET equivalent circuit (from Fig. 8-14) into the circuit for Fig. 10-8. The complete common drain ac equivalent circuit is now shown in Fig. 10-9. The current direction and voltage polarities indicated are those that would occur as the input voltage goes positive.

Input Impedance

Looking into the gate and drain terminals in Fig. 10-9 is the same as looking into the input of a common source amplifier with an unbypassed source resistor (Fig. 10-4). Therefore, the common drain equation for Z_i is derived in exactly the same manner as Eq. 10-2. One important difference between the

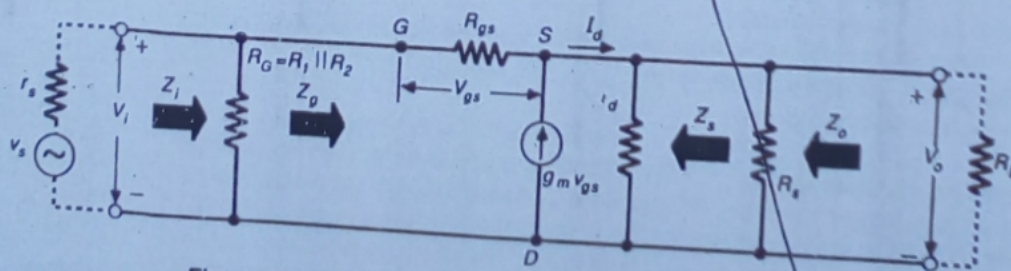
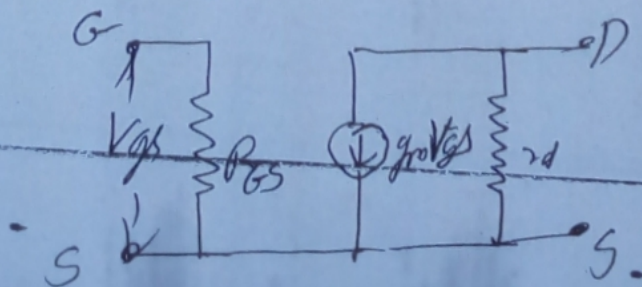


Figure 10-9 The complete equivalent circuit for a common drain amplifier is drawn by substituting the FET equivalent circuit into the ac equivalent circuit of Fig. 10-8.



two circuits is that in the common drain circuit external load resistor R_L appears in parallel with R_S . Thus,

$$Z_g = R_{GS} [1 + g_m (R_S \parallel R_L)] \quad (10-10)$$

As discussed in Section 10-2, this equation gives an extremely large value for Z_g . However, this is important only when the signal source is connected directly in series with the gate terminal to give the highest possible input impedance.

Equation 10-10 gives the input impedance to the FET gate terminal. The circuit input impedance is $R_G \parallel Z_g$, (Fig. 10-9):

$$\begin{aligned} Z_i &= R_G \parallel Z_g \\ &\approx R_G \end{aligned} \quad (10-11)$$

Output Impedance

In the common drain circuit, any variation in output voltage v_o has an effect upon gate-source voltage V_{gs} . To determine the impedance "looking into" the FET source terminal (Fig. 10-9), the signal voltage is assumed to be zero, and the output current $I_s = I_d$ is calculated in terms of the output voltage v_o . With signal voltage $v_s = 0$, v_o is potentially divided across R_{GS} and $r_s \parallel R_G$.

$$V_{gs} = v_o \times \frac{R_{GS}}{(r_s \parallel R_G) + R_{GS}}$$

Normally, $R_{GS} \gg (r_s \parallel R_G)$, so that $V_{gs} \approx v_o$ and

$$I_d = g_m V_{gs}$$

Also,

$$\begin{aligned} Z_s &= \frac{v_o}{I_d} = \frac{V_{gs}}{g_m V_{gs}} \\ Z_s &= 1/g_m \end{aligned} \quad (10-12)$$

Actually, r_d is in parallel with $1/g_m$, but since $r_d \gg (1/g_m)$, it is neglected. Z_s is the output impedance of the device. The circuit output impedance is

$$Z_o = R_S \parallel (1/g_m) \quad (10-13)$$

Typically, $R_S \gg 1/g_m$, and the circuit output impedance is usually taken to be $1/g_m$. For $g_m = 5 \text{ mA/V}$, $Z_o = 200 \Omega$.

Voltage Gain

From Fig. 10-9,

$$v_o = I_d (r_d \parallel R_S \parallel R_L)$$

and

$$I_d = g_m V_{gs}$$

Therefore,

$$v_o = g_m V_{gs} (r_d \parallel R_S \parallel R_L)$$

Again from Fig. 10-9,

$$\begin{aligned} v &= V_{gs} + v_o \\ &= V_{gs} + g_m V_{gs} (r_d \parallel R_S \parallel R_L) \\ A_v &= \frac{v_o}{v_i} \\ &= \frac{g_m (r_d \parallel R_S \parallel R_L)}{1 + g_m (r_d \parallel R_S \parallel R_L)} \end{aligned}$$

Normally, $r_d \gg (R_S \parallel R_L)$, so

$$A_v = \frac{g_m (R_S \parallel R_L)}{1 + g_m (R_S \parallel R_L)} \quad (10-14)$$

So if $g_m (R_S \parallel R_L) \gg 1$,

$$A_v \approx 1$$

There is no minus sign in the equation for the voltage gain of a common drain circuit; when v_i increases, v_o increases.

Example 10-4

The common drain circuit in Fig. 10-7 has $R_1 = 3.9 \text{ M}\Omega$, $R_2 = 2.2 \text{ M}\Omega$, $R_S = 1.5 \text{ k}\Omega$, $R_L = 27 \text{ k}\Omega$. The g_m of the FET is 4 mA/V . Calculate Z_i , Z_o , and A_v .

Solution

From Eq. 10-11,

$$\begin{aligned} Z_i &= R_G = R_1 \parallel R_2 \\ &= 3.9 \text{ M}\Omega \parallel 2.2 \text{ M}\Omega = 1.4 \text{ M}\Omega \end{aligned}$$

From Eq. 10-13,

$$\begin{aligned} Z_o &= R_S \parallel (1/g_m) \\ &= 1.5 \text{ k}\Omega \parallel \left[\frac{1}{4 \text{ mA/V}} \right] = 214 \Omega \end{aligned}$$

From Eq. 10-14,

$$\begin{aligned} A_v &= \frac{g_m (R_S \parallel R_L)}{1 + g_m (R_S \parallel R_L)} \\ &= \frac{(4 \text{ mA/V}) \times (1.5 \text{ k}\Omega \parallel 27 \text{ k}\Omega)}{1 + (4 \text{ mA/V}) \times (1.5 \text{ k}\Omega \parallel 27 \text{ k}\Omega)} \\ &= 0.85 \end{aligned}$$

The common drain circuit in Fig. 10-10 uses a JFET with $g_m = 3000 \mu\text{S}$. **Example 10-5**
Calculate Z_i , Z_o , and A_v .

Solution

$$\begin{aligned} g_m &= 3000 \mu\text{S} \\ &= 3 \text{ mA/V} \end{aligned}$$

From Eq. 10-11,

$$Z_i = 1 \text{ M}\Omega \parallel 1.5 \text{ M}\Omega = 600 \text{ k}\Omega$$

From Eq. 10-13,

$$Z_o = 5.6 \text{ k}\Omega \parallel \left[\frac{1}{3 \text{ mA/V}} \right] = 315 \Omega$$

From Eq. 10-14,

$$\begin{aligned} A_v &= \frac{g_m (R_S \parallel R_L)}{1 + g_m (R_S \parallel R_L)} \\ &= \frac{(3 \text{ mA/V}) \times (5.6 \text{ k}\Omega \parallel 12 \text{ k}\Omega)}{1 + (3 \text{ mA/V}) \times (5.6 \text{ k}\Omega \parallel 12 \text{ k}\Omega)} \\ &\approx 0.92 \end{aligned}$$

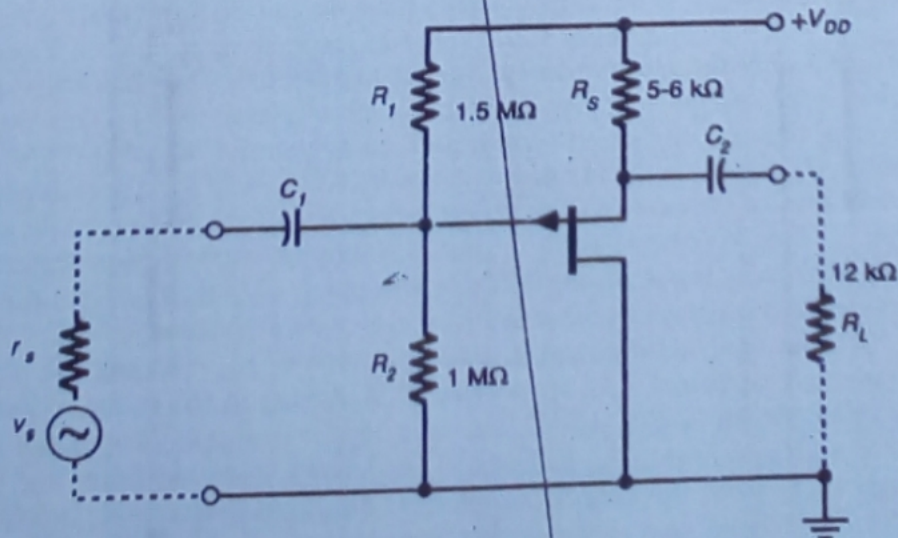


Figure 10-10 Common drain circuit for Example 10-5.

10-6 More Common Drain Circuits

Two common drain circuits using self-bias are shown in Fig. 10-11(a) and (b), one with an n -channel JFET, and the other with a p -channel device. The circuit in Fig. 10-11(a) has its gate biased to ground, while that in Fig. 10-11(b) has $+V_{DD}$ as the gate bias voltage. In both circuits, the input voltage causes V_G to vary and the output (source) voltage follows the input. The ac equivalent circuits and equations in Section 10-5 apply to the circuits in Fig. 10-11, except that $Z_i = R_G$ instead of $R_1 \parallel R_2$.

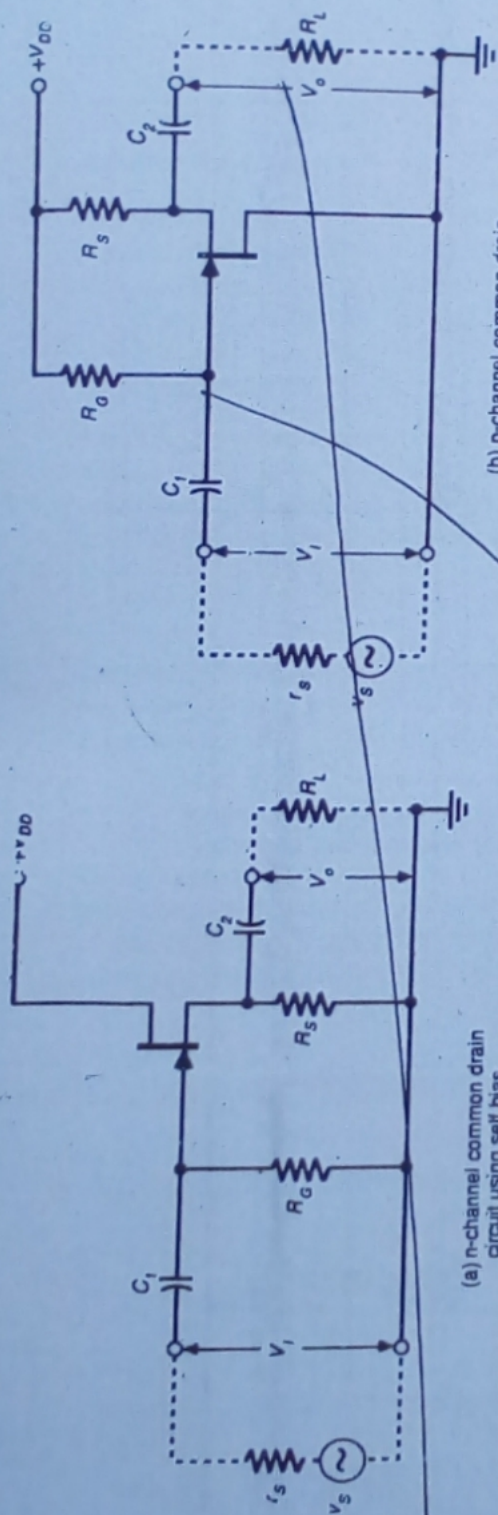
The enhancement MOSFET circuit in Fig. 10-11(c) appears to be using self-bias. But, as discussed in Section 9-6, self-bias is not suitable for MOSFETs. In this case, the difference is that the gate is connected to $+V_{DD}$ via R_G . If the gate were grounded, any voltage drop across R_S would provide a reverse bias at the gate source terminals and thus ensure that the device is biased off. But with $V_G = V_{DD}$, V_{GS} can still be a positive quantity. From a dc point of view, this circuit behaves like a drain-to-gate bias circuit. The ac performance of the circuit is exactly like the performance of the JFET self-bias circuits in Fig. 10-11(a) and (b).

10-7 Common Gate Circuit

The common gate amplifier shown in Figure 10-12 uses a potential divider bias circuit and has an external load resistor R_L capacitor-coupled (via C_3) to the FET drain terminal. The input voltage is coupled to the source terminal via C_2 . Another capacitor C_1 constitutes an ac short circuit from the gate terminal to ground. Because the gate is ac shorted to ground, all of the input voltage at the FET source is developed across the gate-source terminals.

A positive-going input voltage pushes the source terminal in a positive direction while the gate remains at a constant potential. Thus, a positive-going signal increases the negative gate-source bias voltage $-V_{GS}$. This has the effect of reducing the drain current and, consequently, reducing the voltage drop $I_D R_D$ across the drain resistor. Since $V_D = V_{DD} - I_D R_D$, the reduction in I_D results in an increase in (output voltage) V_D . It is seen that a positive-going input produces a positive-going output. Similarly, it can be demonstrated that a negative-going input results in a negative-going output. There is no phase shift between input and output in a common gate amplifier.

The ac equivalent circuit is drawn, as always, by replacing the supply voltage and capacitors with short circuits. Referring to the common gate ac equivalent circuit in Fig. 10-13, it is seen that v_i is applied across the FET source and gate terminals, and that v_o is derived from the drain and gate terminals. Because the gate is common to both input and output, the circuit is termed *common gate* or sometimes *grounded gate*.



(b) p-channel common drain circuit using self bias

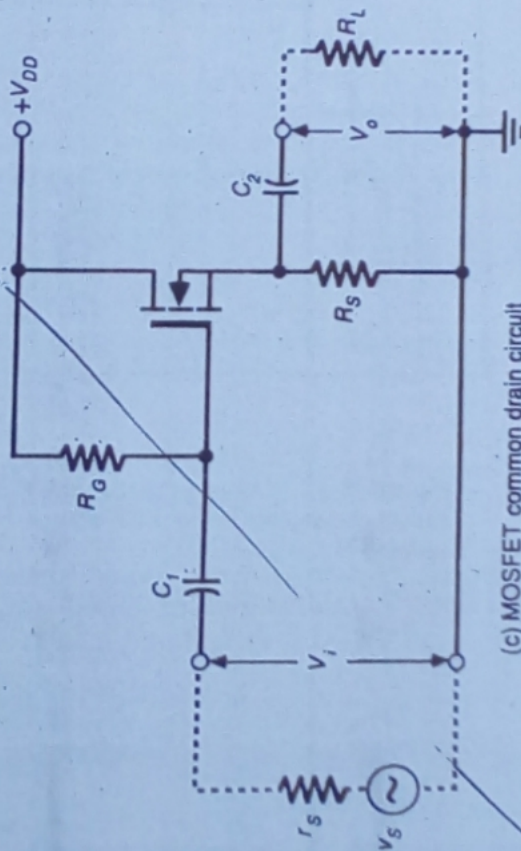


Figure 10-11 More common drain circuits. The ac equivalent circuits for these circuits are similar to that for the FET common drain circuit using potential divider bias.

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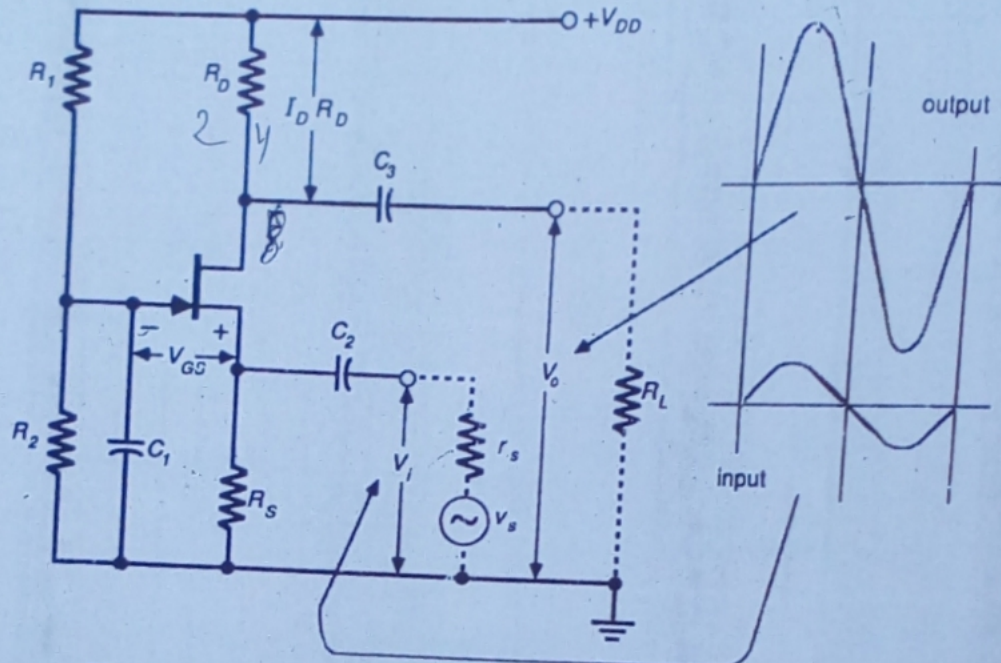


Figure 10-12 Common gate amplifier circuit, showing the signal capacitor-coupled to the FET source terminal and the load capacitor-coupled to the drain.

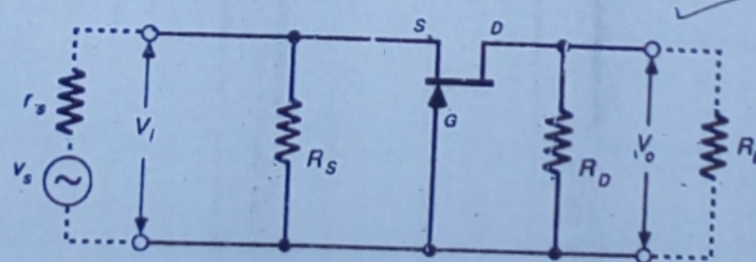


Figure 10-13 The ac equivalent circuit for the common gate amplifier is drawn by replacing supply voltage V_{DD} and all capacitors with short circuits.

10-8 Ac Analysis of Common Gate Circuit

Equivalent Circuit

The complete ac equivalent circuit is drawn by substituting the device equivalent circuit into the ac equivalent circuit of Fig. 10-13. This gives the circuit in Fig. 10-14. Once again, the current direction and voltage polarities indicated are those that would occur as the input voltage goes positive.

Input Impedance

Looking into the source and gate terminals of the common gate equivalent circuit in Fig. 10-14 is the same as looking into the output of a common drain amplifier. The common gate equation for Z_i is thus derived exactly as Eq. (10-12) for the common drain circuit:

$$Z_i = \frac{1}{g_m} \quad (10-15)$$

Just as in the case of the common drain circuit, this equation gives the impedance seen when looking into the FET source terminal. The circuit input impedance is $R_s \parallel Z_i$ (see Fig. 10-14), so

$$Z_i = R_s \parallel \frac{1}{g_m} \quad (10-16)$$

Using a typical g_m of 5 mA/V, it is seen that the input impedance of a common gate circuit is around 200 Ω . Low input impedance is the major disadvantage of this circuit. A consequence of this low input impedance is that the signal voltage v_i is potentially divided across r_s and Z_i (see Fig. 10-14). That is,

$$v_i = \frac{v_s \times Z_i}{r_s + Z_i} \quad (10-17)$$

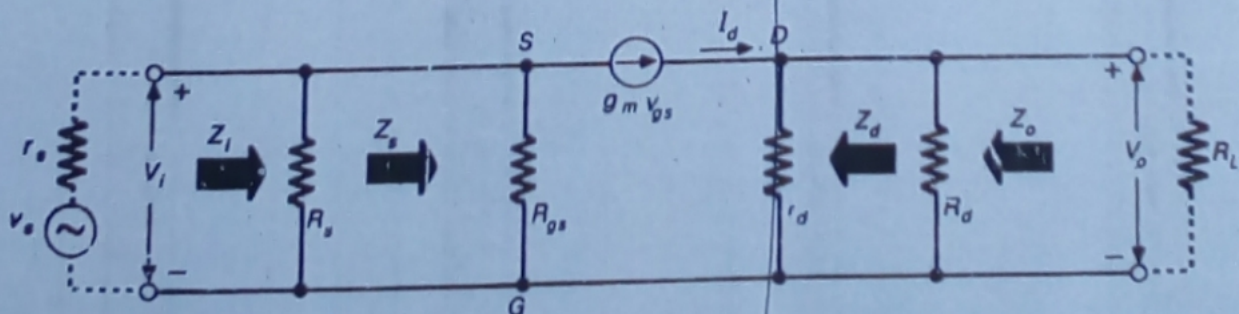


Figure 10-14 The complete equivalent circuit for a common gate amplifier is drawn by substituting the FET equivalent circuit into the ac equivalent circuit of Fig. 10-13.

Eq. 10-17 also applies to common source and common drain circuits. But normally, $Z_i \gg r_s$ for both common source and common drain circuits, so v_i is taken to be equal to v_s . For the common gate circuit, Z_i is usually *not* very much larger than r_s , and so Eq. 10-17 should be employed when calculating the circuit input voltage for a given signal voltage level.

Output Impedance

The output of a common gate circuit is taken from the drain terminal, just as in the case of a common source circuit. So the output impedance at the drain terminal is, once again,

$$Z_d = r_d \quad (10-18)$$

Again, this equation gives the impedance looking into the device drain terminal. The circuit output impedance is

$$Z_o = R_D \parallel Z_d \quad (10-19)$$

Voltage Gain

From Fig. 10-14,

$$v_o = I_d (r_d \parallel R_D \parallel R_L)$$

and

$$I_d = g_m V_i$$

Therefore,

$$v_o = g_m V_i (r_d \parallel R_D \parallel R_L)$$

and

$$A_v = \frac{v_o}{v_i}$$

$$A_v = g_m (r_d \parallel R_D \parallel R_L) \quad (10-20)$$

Usually,

$$r_d \gg (R_D \parallel R_L)$$

so,

$$A_v \approx g_m (R_D \parallel R_L) \quad (10-21)$$

This equation is the same as the equation for the voltage gain of a common source circuit, except that there is no minus sign. As already explained, the output of a common gate circuit is in phase with the input. Like the common source circuit, a typical value of common gate voltage gain is 25.

Example 10-6 The common gate circuit in Fig. 10-12 has $R_1 = 3.9 \text{ M}\Omega$, $R_2 = 2.2 \text{ M}\Omega$, $R_S = 1.5 \text{ k}\Omega$, $R_L = 27 \text{ k}\Omega$, $R_D = 3.3 \text{ k}\Omega$. The FET has $g_m = 3.5 \text{ mA/V}$ and $r_d = 70 \text{ k}\Omega$. Calculate Z_i , Z_o , and A_v . Also, calculate the output voltage when $v_s = 100 \text{ mV}$ and $r_s = 600 \Omega$.